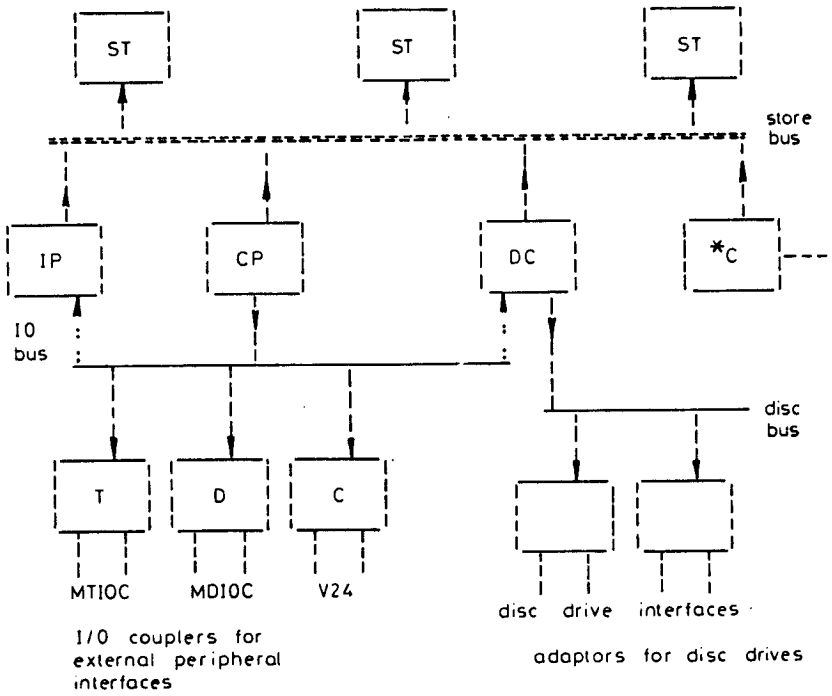

Fig. 1 Basic structure of System 25

Notes
(i) Arrows indicate master/slave relationship
(ii) Dotted lines indicate control information only
(iii) MTIOC etc. explained in text

Key
ST = Store Modules
IP = Instruction Processor
CP = Control Processor
DC = Disc Controller
*C = Other Controllers
T = T Coupler - MTIOC Interface
D = D Coupler = MDIOC Interface
C = C Coupler - Communication Lines

(Multi Device Input Output Channel) allows connection of Point-of-Sale and Factory Data Collection terminals carried over from System Ten.

System 25 also supports a number of local disc drive interfaces which are specific to the particular disc drive; and a variety of communications lines and their associated protocols.

2.2 *System 25 Bus*

The System 25 Bus consists of two main bussed highways – the Store Bus and the I/O Bus – and a subsidiary Disc Bus. There are two lines common to all modules; a

System Reset line and a System Fail line.

The System 25 Bus is tracked in the back plane. The common lines, Store Bus and I/O Bus are tracked to all board locations. The Disc Bus is only tracked to those locations which house a Disc Controller and its associated Disc Adaptors.

On any of the highways, transfers across the highway can only be initiated by a master module. The other module involved in the transfer is a slave module.

2.2.1 Store Bus: The Store Bus is used to transfer either one or five bytes of data between one of the master modules and one of the store modules (a slave module) and consists of

- 23 Address lines (7 bit binary Block Address and a 4 digit decimal Byte Address within a block)
- 40 Bidirectional Data lines (5 bytes)
- 2 Store Function lines
- 1 Store Mode line
- 3 Interface Control lines
- 1 Master Clock line (4 MHz, equivalent to a clock period of 250nsec)

Transfers on the Store Bus occur in synchronism with the Master Clock.

A 'daisy-chain' Bus Request line is used to resolve contention for use of the Store Bus. When a master module obtains access to the Store Bus, it will set Bus Reserved to inhibit the contention logic for one slot time. At the same time the master module enables the address and data onto the bus lines. The store module will respond with data in time to be latched into the master module at the end of the second slot. Thus a single transfer takes two clock periods.

During the second slot contention can take place for the next store cycle.

The store is defined to have two modes of operation. In Word mode, 5 bytes of data are transfered in parallel across the bus. In Byte mode, a multiplexor in the store module is used to transfer a single byte of data on the lowest numbered byte data lines.

The store cycle is 500ns (two clock periods) giving bandwidth of 10Mbyte/s in Word mode and 2Mbytes/s in Byte mode.

2.2.2 I/O Bus: The I/O Bus is driven by the Control Processor (the master module) and is used as the transfer path for control information to other modules and as a byte multiplexing interface for the transfer of data to or from I/O Couplers. It consists of

- 8 Bidirectional data lines
- 2 Function lines
- 2 Function Qualifier lines
- 5 Interface Control lines
- 1 Strobe Line